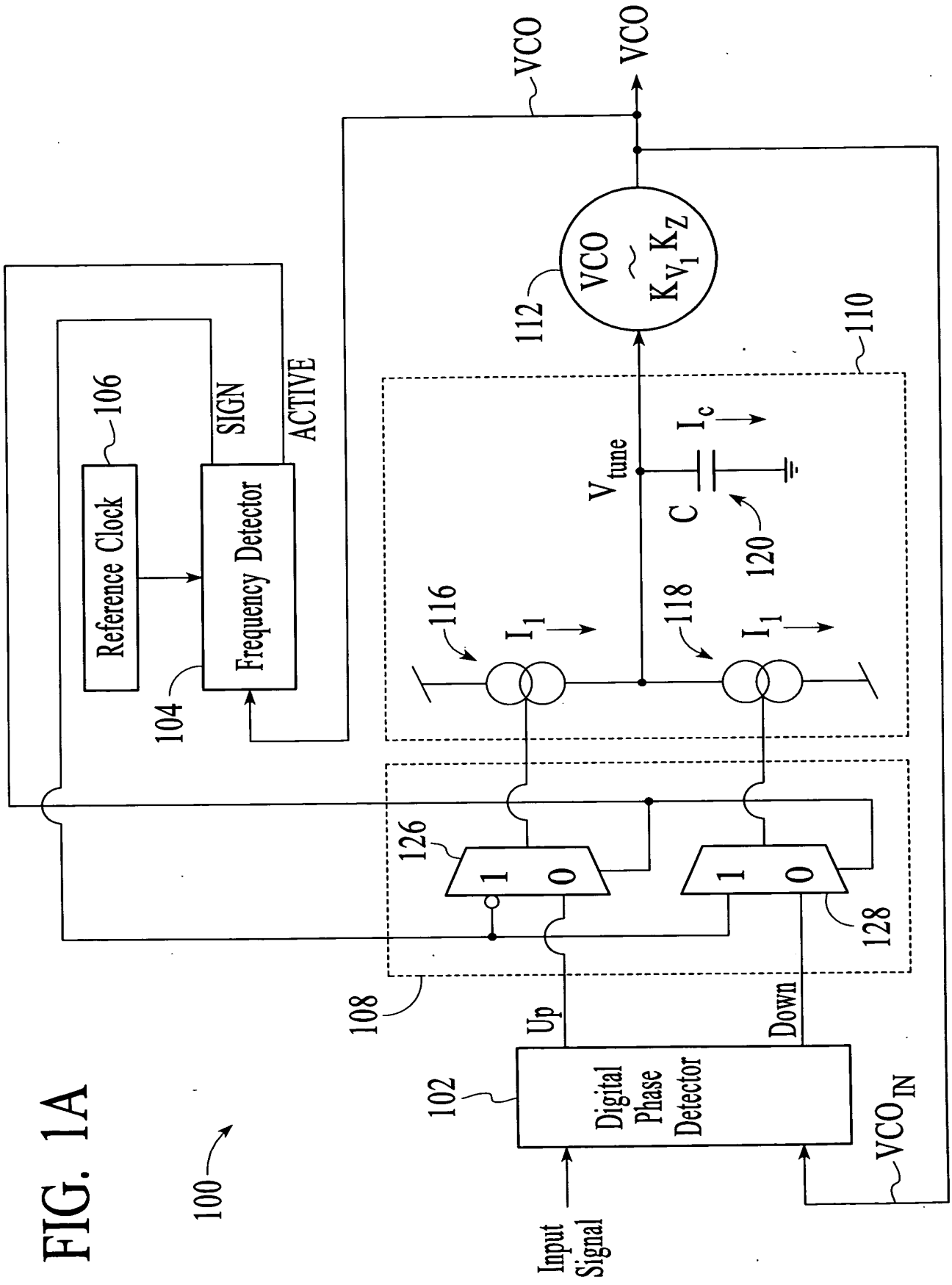
FIG. 1A


100
102
Digital Phase Detector
Input Signal
VCO$_{IN}$
Up
Down
108
126
128
1
0
1
0
110
112
VCO
$K_{V_1}K_Z$
VCO
VCO
116
I_1
118
I_1
V_{tune}
C
I_c
120
104
Frequency Detector
Reference Clock
106
SIGN
ACTIVE

UP	DOWN	SIGN	ACTIVE	I_c
X	X	1	1	$-I_1$
X	X	0	1	$+I_1$
1	0	X	0	$+I_1$
0	1	X	0	$-I_1$

FIG. 1B

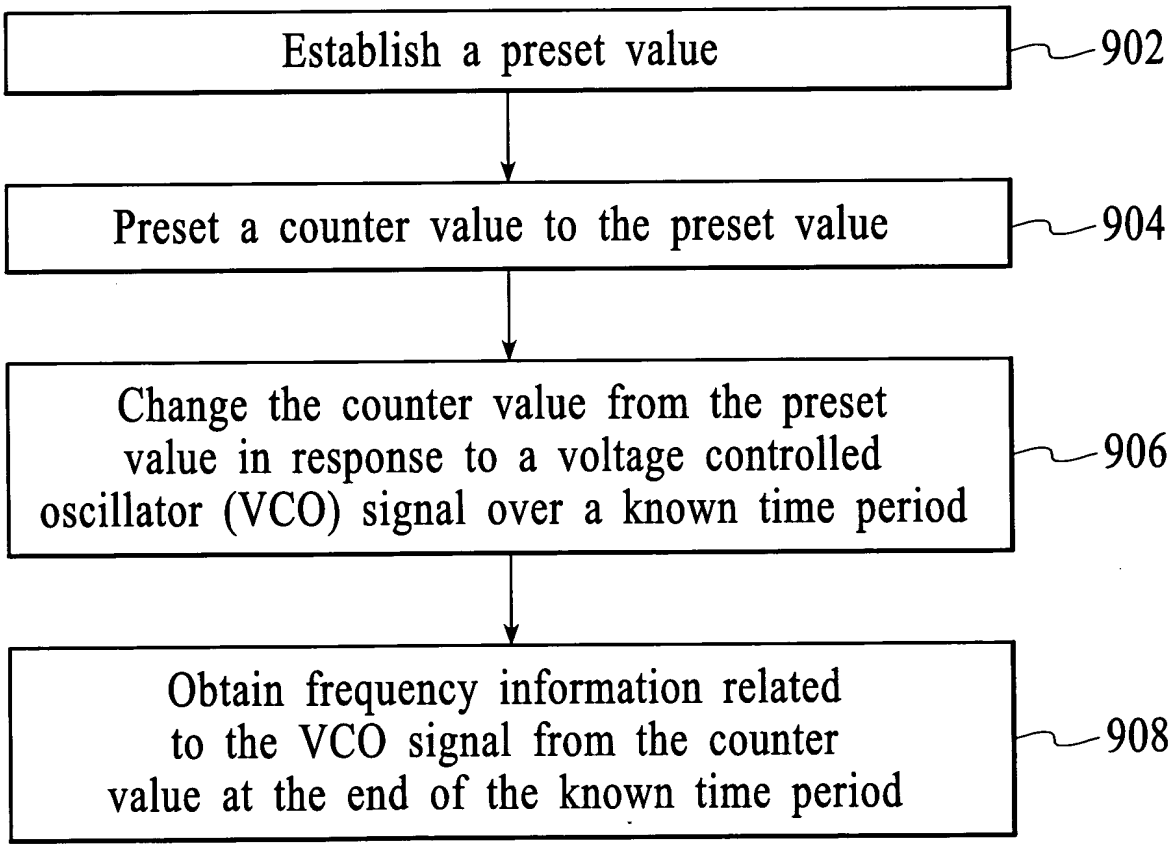


FIG. 9

FIG. 2

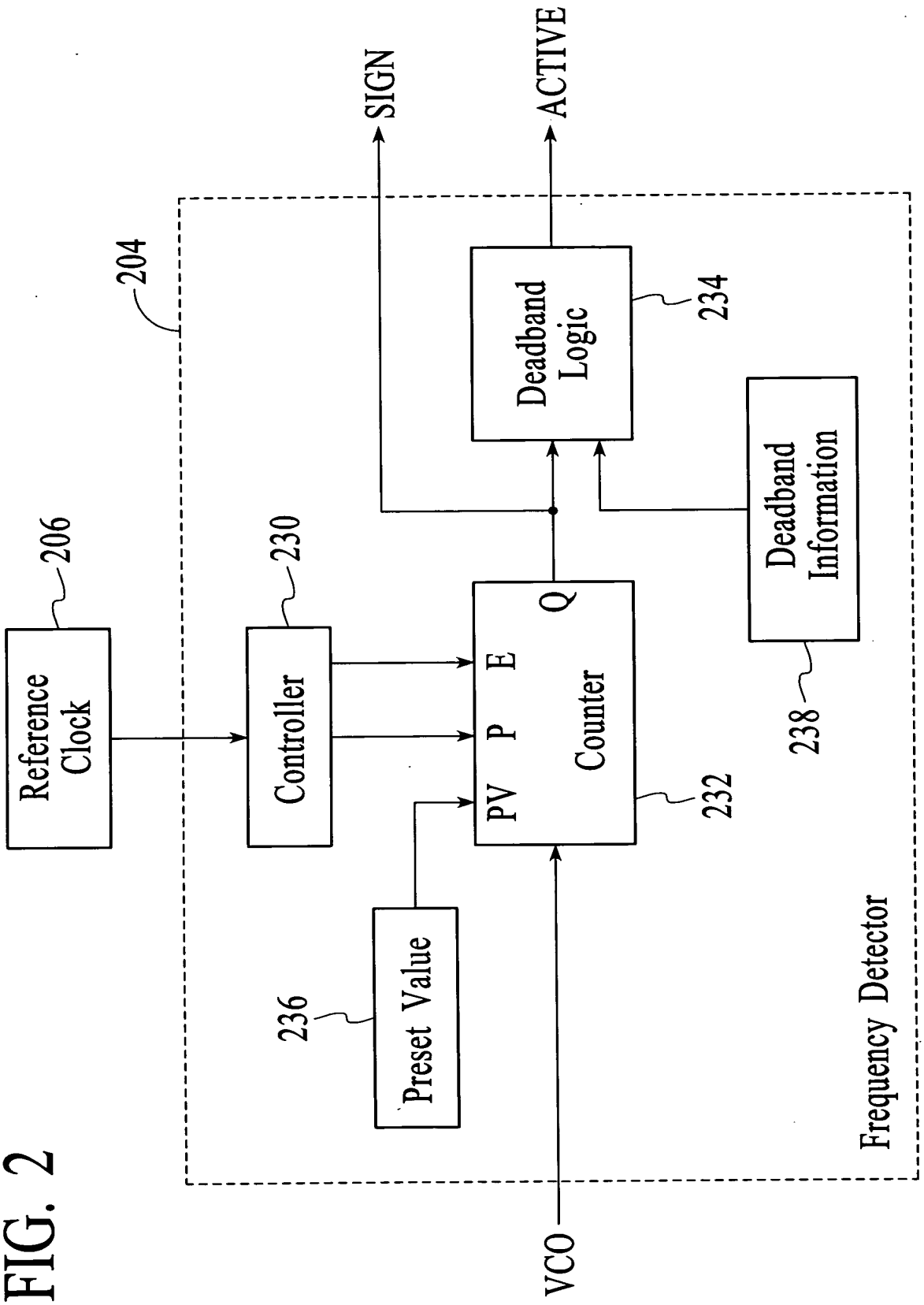
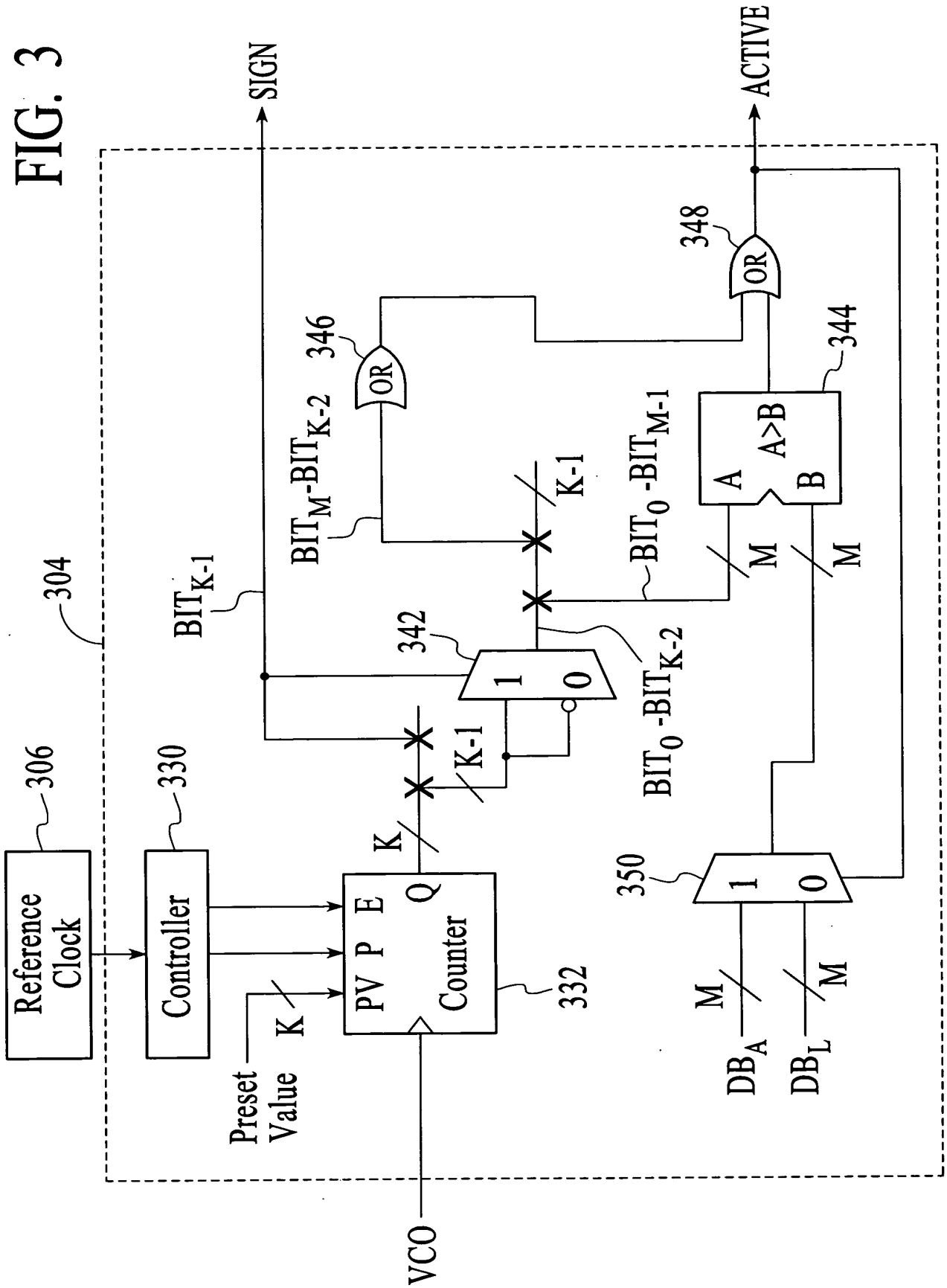

204
SIGN
ACTIVE
Deadband Logic
234
Deadband Information
238
Reference Clock
206
Controller
230
PV P E Q
Counter
232
Preset Value
236
VCO
Frequency Detector

FIG. 3


SIGN
ACTIVE
304
306
330
Reference Clock
Controller
Preset Value
K
PV P E
Q
Counter
332
VCO
K
K-1
342
1
0
BIT$_{K-1}$
BIT$_M$-BIT$_{K-2}$
346
OR
BIT$_0$ -BIT$_{K-2}$
BIT$_0$ -BIT$_{M-1}$
348
OR
344
A
A>B
B
M
M
350
1
0
M
M
DB$_A$
DB$_L$

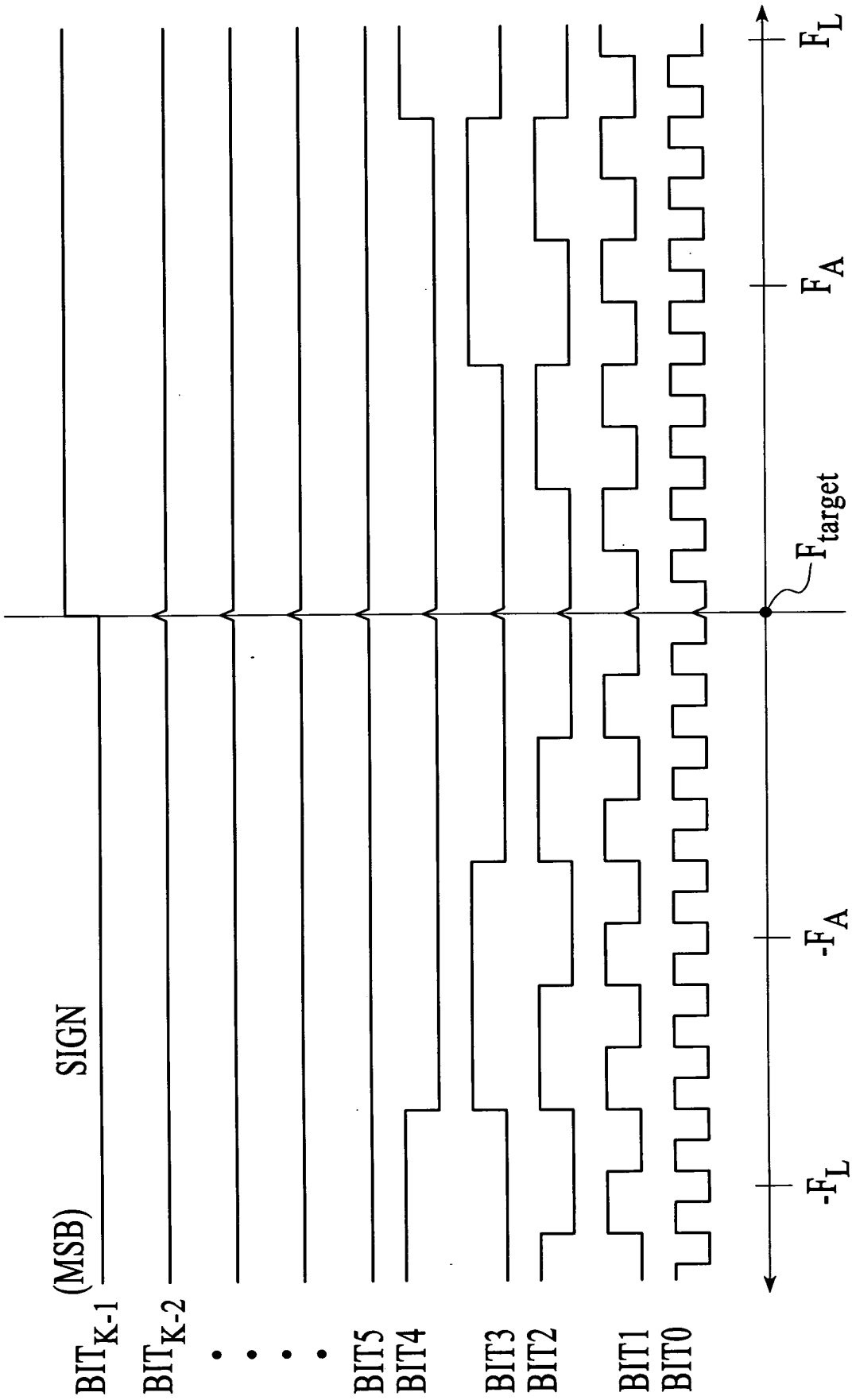

(MSB)
SIGN
BIT$_{K-1}$
BIT$_{K-2}$
BIT5
BIT4
BIT3
BIT2
BIT1
BIT0
F_L
F_A
F_{target}
$-F_A$
$-F_L$

FIG. 4

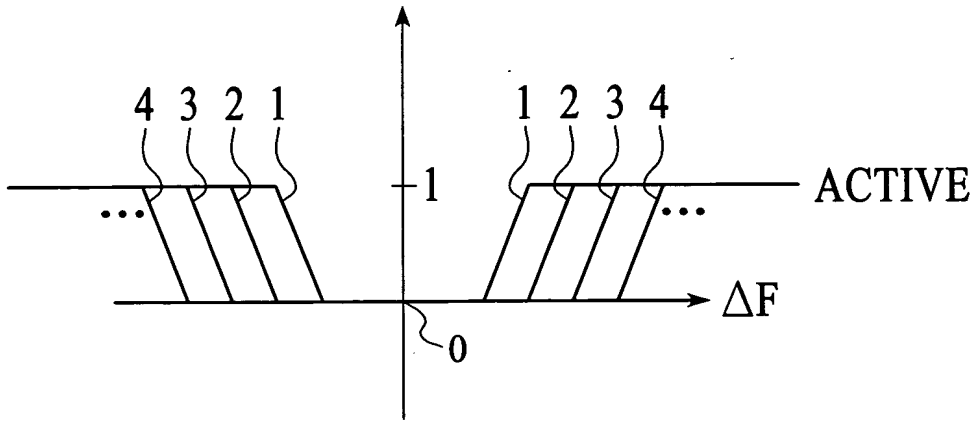


FIG. 5A

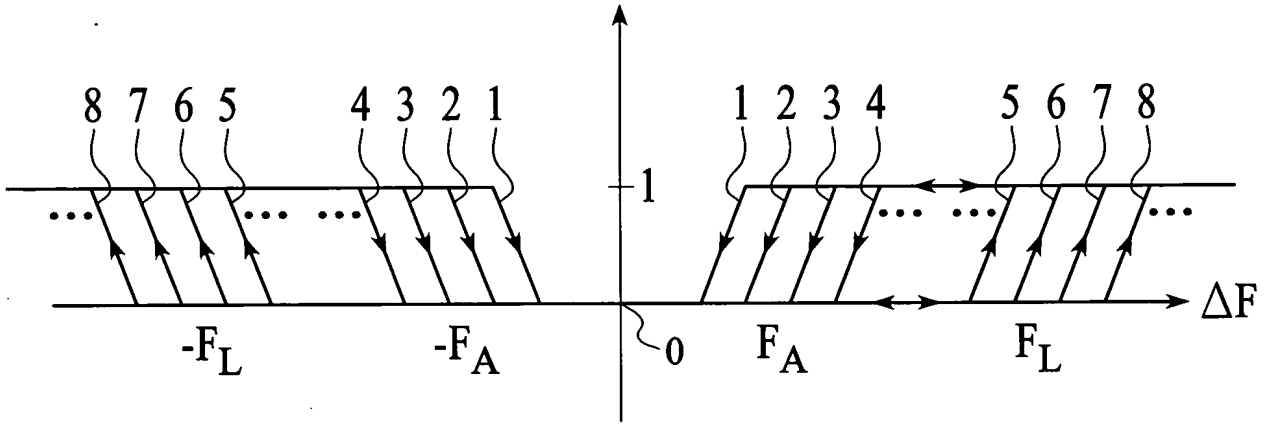


FIG. 5B

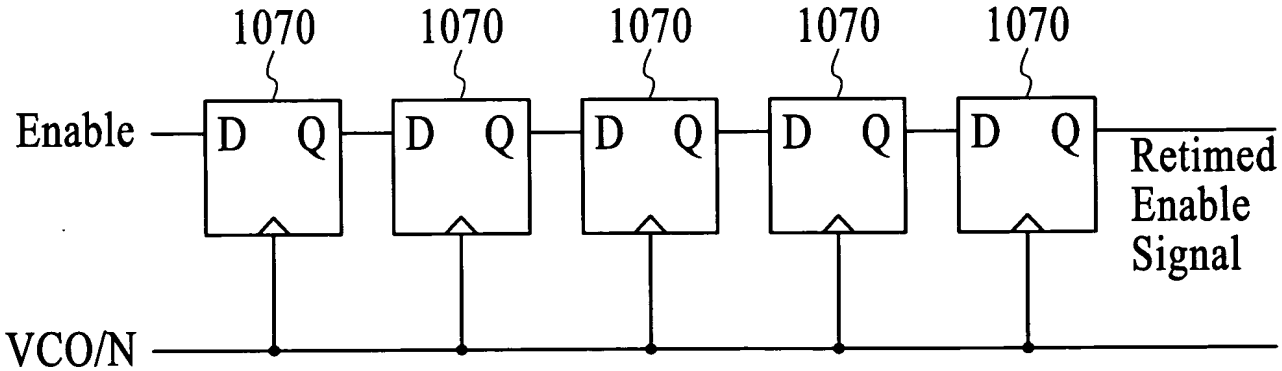


FIG. 10

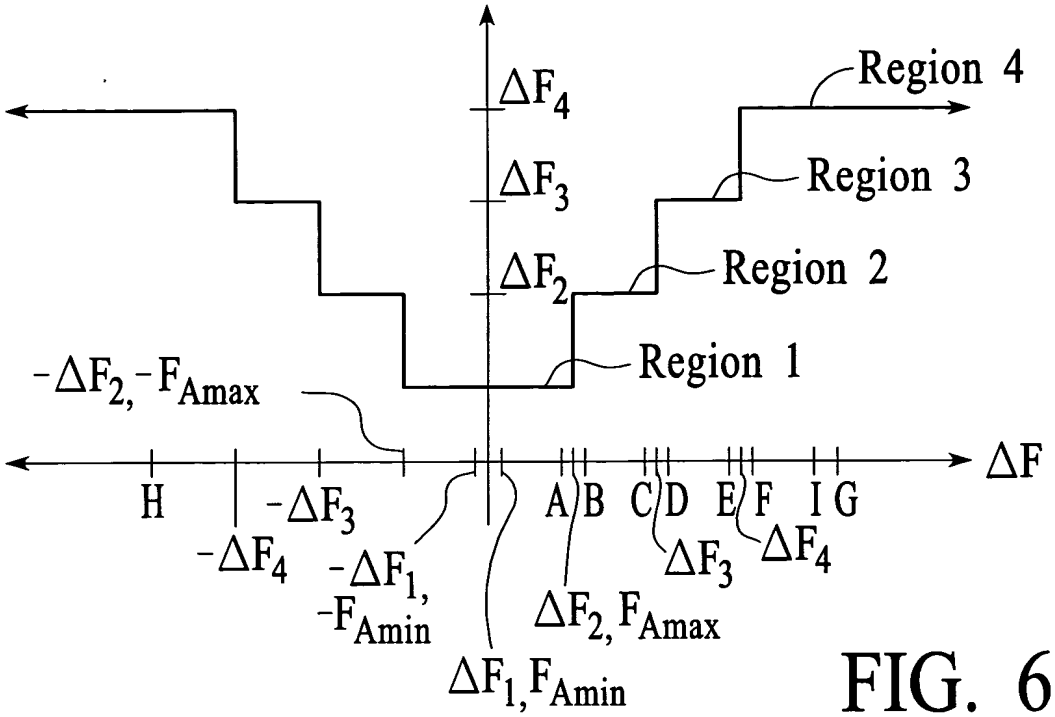

ΔF4
ΔF3
ΔF2
Region 4
Region 3
Region 2
Region 1
-ΔF2, -FAmax
ΔF
H
-ΔF3
-ΔF4
-ΔF1, -FAmin
ΔF1, FAmin
A B C D E F I G
ΔF2, FAmax
ΔF3
ΔF4

FIG. 6

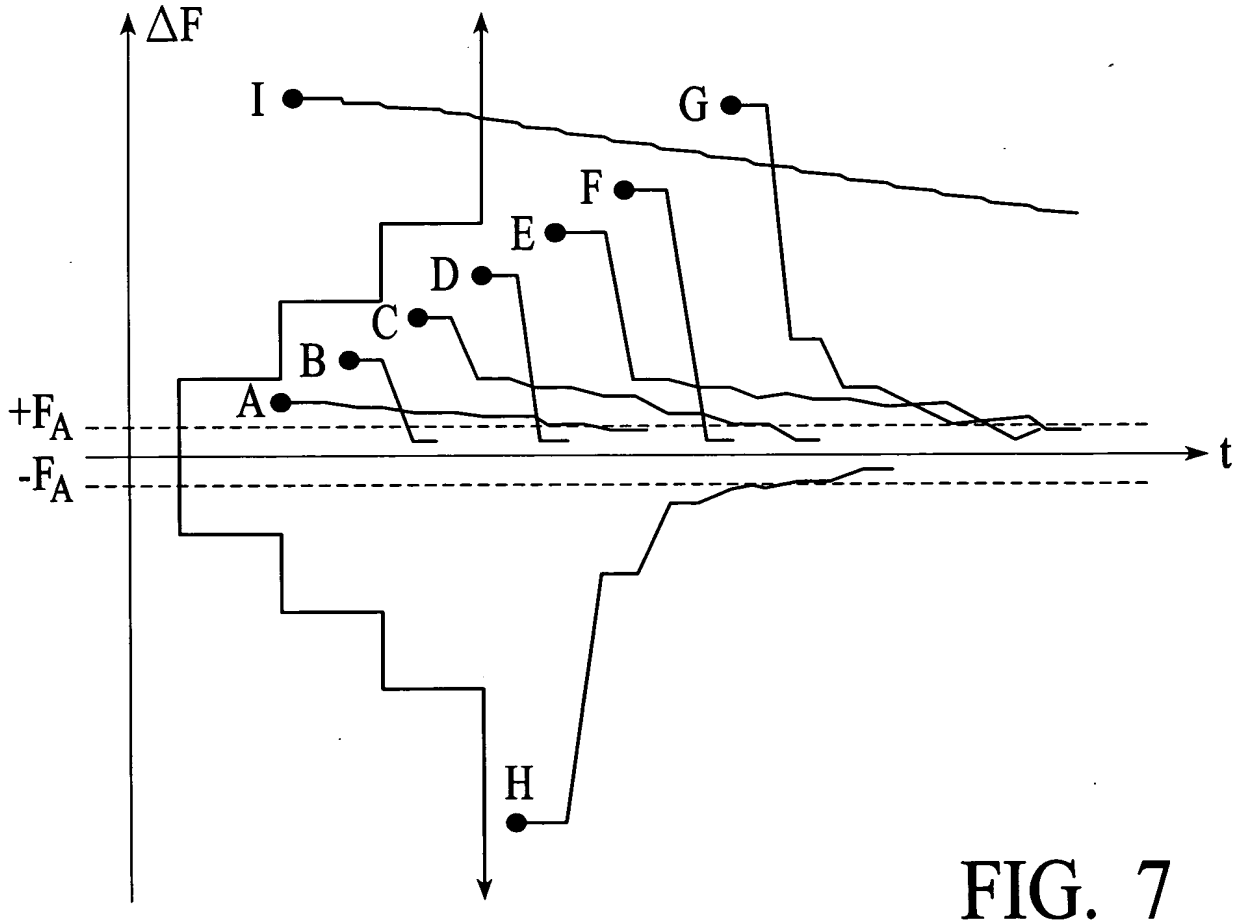

ΔF
I
G
F
E
D
C
B
A
+FA
-FA
t
H

FIG. 7

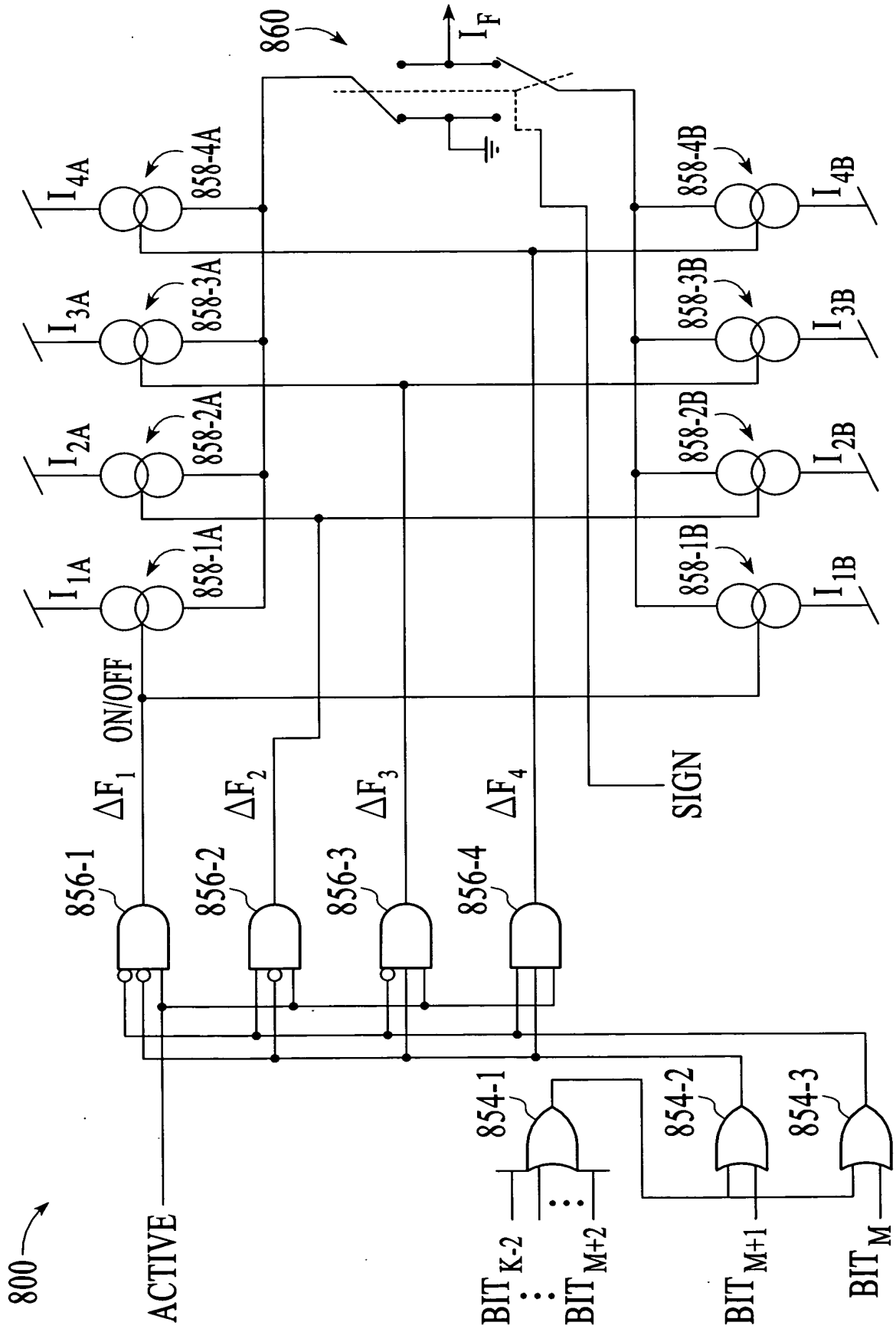

800
ACTIVE
BIT K-2
BIT M+2
BIT M+1
BIT M
From FIG. 3
854-1
854-2
854-3
856-1
856-2
856-3
856-4
ΔF1
ΔF2
ΔF3
ΔF4
ON/OFF
SIGN
858-1A
858-2A
858-3A
858-4A
858-1B
858-2B
858-3B
858-4B
I1A
I2A
I3A
I4A
I1B
I2B
I3B
I4B
860
IF

FIG. 8